Amendments to the Specification:

Please replace the paragraph beginning on page 2, line 14 with the following amended paragraph:

Memory chips are known that employ a double data rate (DDR) communication scheme. Such a memory may be used in any suitable apparatus including, for example, a graphics acceleration system employing one or more graphics chips that ~~sending~~ send information to and retrieve data from a memory, such as a frame buffer. Memory interface circuits for facilitating a double data rate communication scheme are also known.

Please replace the paragraph beginning on page 3, line 4 with the following amended paragraph:

In receiving mode, when the graphics chip or other circuit is receiving data from memory, the memory chip generates and sends the STROBE and DATA signals back. However, typical double data rate interface requirements require the memory chip to send the STROBE and DATA signals simultaneously to simplify the on board memory chip circuitry. Accordingly, a receiving circuit, such as a graphics chip or other suitable circuit, has to delay internally, the received STROBE signal that was sent from the memory chip to provide the same conditions for the receiving circuit input flip flop as for the sending circuits. In other words, the received STROBE signal that is actually [[is]] the clock input of the graphics chip flip flop has to be in the middle of the data signal window. This time offset has to be stable, including over temperature changes, voltage changes and fabrication process variations.

Please replace the paragraph beginning on page 5, line 30 with the following amended paragraph:

A signal phase shifting circuit [[is]] shifts the phase of an input signal, such as a STROBE signal, based on a reference signal, such as a CLOCK signal, to facilitate, for example, receiving of double data rate data. The signal phase shifting circuit includes a

reference signal period dividing circuit having a feedback delay matching array operatively coupled to one of a plurality of voltage control delay lines (VCDL). The signal phase shifting circuit also includes a variable delay circuit that provides a phase shifted output signal, such as a phase shifted STROBE signal, that includes a delay stage and a phase shifted output signal drive buffer coupled to the delay stage, such as a voltage control delay line. The feedback delay matching array includes a plurality of serially coupled buffer stages operatively coupled to compensate for delay variations associated with the phase shifted output signal drive buffer in the variable delay circuit. Accordingly, a more stable STROBE signal phase shift occurs that is less sensitive to temperature and voltage variations while still allowing the compensation of delay due to, for example, printed circuit board layout delays and other delays.